Mercury ADC Circuit Description
Revision: 1
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1. Applicability

This document applies to Mercury Main Board schematic 03-925060-00, Revision PR4.

2. System description

The central ADC system consists of a 16-bit ADC, several voltage references, a programmable-gain amplifier (PGA), a group of analog multiplexers, excitation circuitry for the RTD temperature probes, a barometric absolute pressure sensor, and timing logic to control the system. The logic, which relieves software of any precise timing requirements, is contained in FPGA X2.

3. ADC

The ADC is a 16-bit (or 15-bit plus sign) delta-sigma converter. The excellent noise-rejecting characteristics of this conversion technique allow consistent noise levels below ±1/2LSB with the simple supply filtering networks of R53, C59, R81, and C57. The clock frequency at XIN is 320kHz.

Conversions are started 160 times per second by a hardware-generated pulse on pin 2. A conversion takes 5 milliseconds, after which DRDY\ goes low, generating an interrupt and latching a new, buffered value of BP/UP\ (bipolar/unipolar mode). Software then has over 6 milliseconds to read the converted value and update the buffer holding the next desired value of BP/UP\, before the data from the next conversion will be ready. The converted value is read serially from SDATA, with hardware sending a pulse to SCLK each time SDATA is read, thus shifting out the next bit. When all of the bits have been read, DRDY\ goes high again.

The differential input range of the ADC in unipolar mode is equal to the voltage difference between VREF+ and VREF-, or 2.5V. Since the converter is supplied from +5.25V only, the analog input zero level must be shifted up above ground if negative values are to be converted in bipolar mode. AIN- is connected to +2.5V, so the input range at AIN+ in unipolar mode is +2.5V to +5.0V, and the range in bipolar mode is 0V to +5V. Resistors R51, R54, and R55 shift and attenuate the ±10V levels from the PGA output to cover the 0 to +5V input range of the ADC. R50, C60, and C63 smooth the input charge packets which are transferred when the ADC samples its input.

4. Programmable-gain amplifier and references

Gains of 1, 2, 4, 8, 16, 32, and 64 are provided by the programmable-gain amplifier. Corresponding full-scale voltages for the ADC, measured at the PGA input, range from 10V down to 156mV (nominal). Resolution depends upon the conversion mode, ranging from 160μV to 2.5μV in unipolar mode, or 320μV to 5μV in bipolar mode (nominal). The gain-setting resistors in network R4 have only 1% tolerance, so the overall gain (including R51, R54, and R55) is set slightly low to ensure that the nominal full-scale inputs can be converted without clipping. Similarly, the ADC input voltage with zero volts into the PGA is set slightly above 2.5V, so that PGA inputs all the way down to ground can always be digitized, regardless of component tolerance variations.

Capacitor C62 reduces high-frequency noise from the amplifier, while C50 and C54 suppress digitally-induced noise. R43 limits the current pulse which is drawn from the input voltage source when the input multiplexer switches, charging C50 to a new voltage. The time constants set by these capacitors are short enough to settle to the required accuracy much more quickly than the 1ms which is available between conversions. In addition, the input multiplexer is set to ground for 200μs after each conversion. This elminates any residual crosstalk between channels which might occur if the amplifier is driven into saturation. *Note: the muiltiplexer is set to ground by hardware, so this action cannot be stopped by holding the multiplexer setting at a fixed channel in software. Voltmeter readings at the output of the muxtiplexer will be about 3% lower than at the input in this case.*

There are three precision reference voltages: +10V, +5V, and +2.5V. The basic accuracy of the +10V reference (U9) is ±0.1%. C13 minimizes the glitches on the reference induced by the DAC switches, which operate asynchronously to the ADC conversions. The other two values are divided down from this reference by resistors in network R4 which have ±0.1% ratio accuracy, giving guaranteed accuracies of ±0.2% for the +5V and +2.5V references. One half of AR5 buffers the +2.5V reference for the ADC. The other half of AR5, along with Q1, can supply up to 40mA of excitation current at +5V to the RTDs, the barometric absolute pressure transducer, and the EFC modules.

The remaining references voltages (+0.625V and +0.156V) have low precision and stability, being generated by a resistive divider of 1% resistors (R39, R41, and R42). These voltages are used only as transfer standards for calibrating the higher gains of the PGA. Calibration begins by reading the +10V reference on gain 1 and proceeding to higher gains and lower reference voltages. Each reference is measured at a lower gain, which has already been calibrated, immediately before being used to calibrate higher gains, so high accuracy and stability are not needed.

5. Multiplexers and input sources

The primary input multiplexer, U16, at the input of the PGA can handle the ±10V signals from the detectors and the +10V reference. All of the remaining signals are scaled to ± 5V or less, and are selected by the secondary multiplexers (U4, U10, and U15) which

connect to inputs of U16. The secondary multiplexers are less expensive devices which cannot handle voltages exceeding ±5V.

While the multiplexer channel is selected by software, the actual value output to lines MMUX0-5 is double-buffered and delayed by hardware. Like the BP/UP\ signal mentioned above, the value in the output latch which drives the multiplexers is loaded from a buffer when DRDY\ goes low. This setting is then used for the next conversion about 1ms later. Software reloads the buffer during the interrupt routine, which is triggered by DRDY\, with the value needed for the conversion after the next one.

The RTD probes are excited from the +5V reference through 1K±0.1% resistors. Current through the RTDs varies between 4 and 5mA over the measured temperature range. One section of the excitation resistor network (R3) feeds a fixed resistor, R40. This is used to verify the operation of the complete temperature measurement circuit by reading this ADC channel during run time.

The RAM backup battery voltage is read through resistor R38, which limits the discharge current when the power is off. (Negligible current is drawn when multiplexer U10 has power applied.) C42 reduces the noise which is picked up due to the very high source resistance of R38.

The barometric absolute pressure sensor (MP1 on schematic sheet 1) is used to compensate the electronic flow control system for changes in barometric pressure. Its output voltage at pin 1 depends upon the reference voltage at pin3 and the absolute pressure according to the following formula:

$$V_{out} = V_{ref} * (.009 * P - .095),$$

where P is in kilopascals, and voltages are in volts. Normal atmospheric pressure at sea level is about 103kPa, and the reference voltage is 5 volts, so the expected value of V_{out} under these conditions would be about 4.6V. Atmospheric pressure usually remains within 3% of its nominal value with changes in weather, but decreases by about 3.4kPA for each thousand feet increase in elevation. Thus, voltage readings at pin 1 of MP1 should be between 4.4 and 4.8V at sea level, decreasing by 150mV per thousand feet of elevation above sea level.

Proper operation of the ADC, PGA, and two of the input multiplexers is guaranteed by a successful self-calibration. However, this procedure could not detect a failure of the +10V reference. For this reason, the +5V digital supply voltage is read through multiplexer U10. Reference operation is tested, but precision is not, since the test is good only to ±5%. Reading the -5V supply through the same multiplexer guarantees that a power supply failure could not cause erroneous readings.

6. Log of revisions and file identification

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